RM-60

DEBUG AND VIDEO QUEUE FOR MULTI-PROCESSOR CHIP

ABSTRACT OF THE DISCLOSURE

A microprocessor die contains several processor cores and a shared cache. Trigger conditions for one or more of the processor cores are programmed into debug registers. When a trigger is detected, a trace record is generated and loaded into a debug queue on the microprocessor die. Several trace records from different processor cores can be rapidly generated and loaded into the debug queue. The external interface cannot transfer these trace records to an external in-circuit emulator (ICE) at the rate generated. The debug queue transfers trace records to the external ICE using a dedicated bus to the ICE so that bandwidth is not taken from the memory bus. The memory bus is not slowed for debugging, providing a more realistic debugging session. The debug buffer is also used as a video FIFO for buffering pixels for display on a monitor. The dedicated bus is connected to an external DAC rather than to the external ICE when debugging is not being performed.